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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,928	12/12/2003	Alexander Kalnitsky	55123P231D	2239

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,928	KALNITSKY ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In view of the amendments received 2 March 2005, the restriction of 4 February 2005 is withdrawn.

Drawings

The drawings were received on 13 December 2004. These drawings are acceptable for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23-37, 47, 49, 50, 53, 54 are rejected under 35 U.S.C. 102(e) as being anticipated by Kalnitsky et al., US Patent No. 6,492,237 B2, from the IDS.

Kalnitsky anticipates a bipolar transistor, comprising: in fig. 2D,

a substrate having a collector region 204, the collector region being a collector terminal, where the electrons collect; a plurality of mono-crystalline layer with the lower portion of 206 being the first epitaxial layer and the upper portion of 206 being the second epitaxial layer, a first epitaxial silicon layer having a mono crystalline portion 206A, on a mono-crystalline portion of the substrate; an emitter stack 220 on the first epitaxial silicon layer, the emitter stack being an emitter terminal, where electrons are inputted into the device; a second epitaxial silicon layer 206B having a mono- crystalline portion on the mono-crystalline portion of the first epitaxial silicon layer, bottom portion of 206, located outside the emitter stack, wherein 206B does not contact 220; wherein a region of the first epitaxial silicon layer located under the emitter stack is an intrinsic base region 206A and a region of the second epitaxial silicon layer 206B on portions of the first epitaxial silicon layer located outside the emitter stack being a raised extrinsic base region; wherein the raised extrinsic base region has a thickness greater than a thickness of the intrinsic base region; and wherein the intrinsic base region and the raised extrinsic base region provide a base terminal of the bipolar transistor with lower resistivity, do extrinsic doping,

limitations from claims 23, 33, wherein the extrinsic base region has a thickness x, thickness at label 206B, and the intrinsic base region has a thickness y, thickness at label 206A, and wherein x is greater than y, col. 5, line 24 - col. 6, line 28;

limitations from claims 24, 36, 37, the bipolar transistor, in fig. 2D, wherein the emitter structure includes a polysilicon emitter having a first portion with a width a, region of 220 between 228, a second portion with a width b, region of 220

a, region of 220 between 228, a second portion with a width b, region of 220 between 214, and a third portion with a width c, region of 220 above 214; wherein c is greater than b which is greater than a; and wherein the first portion defines an emitter base junction, and wherein the third portion defines an emitter contact region, col. 6, lines 1-14;

limitations from claim 25, the bipolar transistor, in fig. 2D, 212, wherein the emitter region structure further includes nitride spacer directly adjacent to the polysilicon emitter 220, col. 5, lines 24-39;

limitations from claim 26, the bipolar transistor, wherein the extrinsic base region comprises: in fig. 2D, a first epitaxial layer, lower portion of layer 206; and a second epitaxial layer, upper portion of layer 206 on the first epitaxial layer;

limitations from claim 27, the bipolar transistor, wherein the first epitaxial layer is a SiGe epitaxial layer and the second epitaxial layer is a heavily p-type doped Si or SiGe epitaxial layer: col. 3, lines 42-51;

limitations from claims 28, 32, 53, 54; the bipolar transistor, wherein the bipolar transistor is an npn transistor, col. 3, line 26-29;

limitations from claim 30, 54, the bipolar transistor, in fig. 1A, lower portion or 106, wherein the first epitaxial layer is a p-type Si, SiGe or SiGe:C epitaxial layer and the second epitaxial layer is a selectively deposited heavily p-type doped Si epitaxial layer or a selectively deposited heavily p-type doped SiGe epitaxial layer, col. 3, lines 42-51, wherein 'heavily doped' is subjective to the observer;

limitations from claim 31, the bipolar transistor, in fig. 2C, wherein the emitter stack includes a first nitride layer 212 having an emitter window, gap labeled 220, and, in fig. 2D, a polysilicon emitter within the emitter window, 220;

limitations from claim 34, the bipolar transistor, in fig. 2D, wherein the extrinsic base region 206D, is raised relative to the intrinsic base region 206A;

limitations from claim 35, the bipolar transistor, in fig. 2D, wherein the polysilicon emitter structure has a first portion providing an emitter base junction, region of 220 between 228, a second portion providing conduction, region of 220 between 214, and a third portion providing an emitter contact region, region of 220 above 214, col. 5, line 40 - col. 6, line 20;

limitations from claim 49, the bipolar transistor, in fig. 2D, wherein at least a second epitaxial layer, upper portion of 206, of the plurality of epitaxial layers is coupled to the first epitaxial layer, lower portion of 206 to provide the raised extrinsic base;

limitations from claim 50, the bipolar transistor, wherein the first epitaxial layer, lower portion of 206, is a SiGe epitaxial layer and the at least second epitaxial layer is a heavily p-type doped Si or SiGe epitaxial layer, upper portion of 206, col. 3, lines 42-51.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 38, 39, 41, 42, 44, 45, 51, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalnitsky as applied to claims 23-37, 47, 49, 50, 53, 54 above, and further in view of Konig et al., US Patent No. 5,587,327.

Kalnitsky does not specify using polycrystalline regions in the base regions, but Konig does. Konig teaches a bipolar transistor, in fig. 1D, substrate 1, collector region 2, oxide layer 4, col. 3, lines 30-45,

limitations from claim 38, the bipolar transistor, in fig. 1F, wherein the extrinsic base region 8B, further has a polycrystalline portion over an oxide layer 4 of the substrate, col. 4, lines 17-34;

limitations from claims 39, 51, the bipolar transistor, further comprising: in fig. 1G, a silicide layer on 12 a top surface of the extrinsic base region, here labeled 14 to lower a contact resistance, col. 4, lines 7-34;

limitations from claim 41, the bipolar transistor, in fig. 1E, wherein the first epitaxial layer further has a poly-crystalline portion 7B, on an oxide layer 4 of the substrate, and the second epitaxial layer further has a has a poly-crystalline portion, 9B on the poly-crystalline portion of the first epitaxial layer, col. 3, lines 54-65;

limitations from claim 42, the bipolar transistor, further comprising: in fig. 1G, a silicide layer 12 on a top surface of the second epitaxial silicon layer 14 to lower a contact resistance, col. 4, lines 7-34;

limitations from claim 44, the bipolar transistor, in fig. 1G, wherein the extrinsic base region further has a poly crystalline portion over an oxide layer of the substrate, col. 3, lines 54-65;

limitations from claim 45, the bipolar transistor, further comprising: a silicide layer on a top surface of the extrinsic base region to lower a contact resistance, col. 4, lines 7-34. Konig gives motivation in col. 1, lines 19-51. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Konig's process with Kalnitsky's invention would have been beneficial because it produces maximum frequency properties with simple preparation.

Claims 40, 43, 46, 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalnitsky in view of Konig as applied to claims 23-39, 41, 42, 44, 45, 47, 48-51, 53, 54 above, and further in view of Wolf, V. I, pp. 399-400.

Neither Kalnitsky nor Konig specify using a $CoSi_2$ or $TiSi_2$, but Wolf does. Wolf in p. 399, bottom paragraph and Table 5, lists the use of $TiSi_2$ and gives motivation. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Wolf's process with Kalnitsky's and Konig's invention would have been beneficial because refractory metal silicides are able to withstand higher temperatures and have low resistivities.

Response to Arguments

Applicant's arguments with respect to 23-37 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

21 April 2005
WB